

FIG. 1
ARCHITECTURE

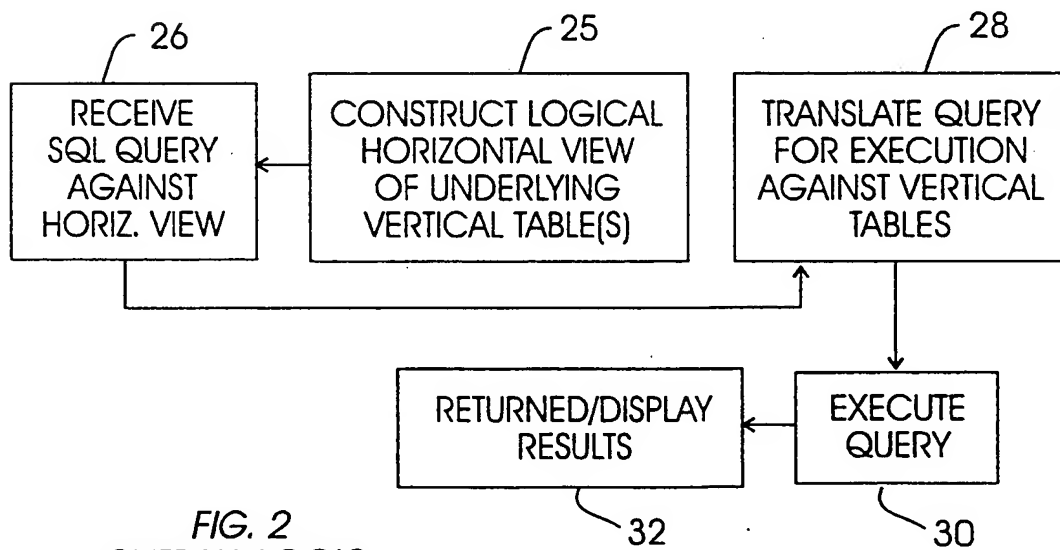


FIG. 2
OVERALL LOGIC